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1   A VLIW architecture for a trace scheduling compiler   ◪

Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman
October 1987 **ACM SIGARCH Computer Architecture News , ACM SIGPLAN Notices ,
ACM SIGOPS Operating Systems Review , Proceedings of the second
international conference on Architectual support for programming
languages and operating systems ASPLOS-II**, Volume 15 , 22 , 21 Issue 5 , 10 , 4
Publisher: IEEE Computer Society Press, ACM Press

Full text available: 📄 pdf(1.59 MB)   Additional Information: full citation, abstract, references, citings, index terms

> Very Long Instruction Word (VLIW) architectures were promised to deliver far more than
> the factor of two or three that current architectures achieve from overlapped execution.
> Using a new type of compiler which compacts ordinary sequential code into long
> instruction words, a VLIW machine was expected to provide from ten to thirty times the
> performance of a more conventional machine built of the same implementation
> technology.Multiflow Computer, Inc., has now built a VLIW called the TRACE™< ...

2   GASS: a data movement and access service for wide area computing systems   ◪

Joseph Bester, Ian Foster, Carl Kesselman, Jean Tedesco, Steven Tuecke
May 1999 **Proceedings of the sixth workshop on I/O in parallel and distributed
systems**
Publisher: ACM Press
Full text available: 📄 pdf(950.99 KB)   Additional Information: full citation, references, citings, index terms

3   Status report of the graphic standards planning committee   ◪

Computer Graphics staff
. August 1979 **ACM SIGGRAPH Computer Graphics**, Volume 13 Issue 3
Publisher: ACM Press
Full text available: 📄 pdf(15.01 MB)   Additional Information: full citation, references, citings

4   Special issue: AI in engineering   ◪

D. Sriram, R. Joobbani
April 1985 **ACM SIGART Bulletin**, Issue 92
Publisher: ACM Press

Full text available: ⬚ pdf(8.79 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>

The papers in this special issue were compiled from responses to the announcement in the July 1984 issue of the SIGART newsletter and notices posted over the ARPAnet. The interest being shown in this area is reflected in the sixty papers received from over six countries. About half the papers were received over the computer network.

5 A survey of commercial parallel processors
Edward Gehringer, Janne Abullarade, Michael H. Gulyn
September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4
Publisher: ACM Press
Full text available: ⬚ pdf(2.96 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>citings</u>, <u>index terms</u>

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share ...

6 Operational features of a MOS timing simulator
P. Kozak, H. K. Gummel, B. R. Chawla
June 1988 **Papers on Twenty-five years of electronic design automation**
Publisher: ACM Press
Full text available: ⬚ pdf(657.10 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

7 A framework for the assessment of operating systems for small computers
Hossein Saiedian, Munib Siddiqi
April 1996 **ACM SIGICE Bulletin**, Volume 21 Issue 4
Publisher: ACM Press
Full text available: ⬚ pdf(1.89 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

A number of high performance operating systems are now available for small computers on different hardware platforms. These operating systems offer many advanced features formerly reserved for their workstation and minicomputer counterparts. This article surveys the most widely used of such operating systems, namely OS/2, Windows NT, Linux and Macintosh System 7.5. It provides an account on the history, design objectives and evolution of these operating systems and discusses their key features, ...

Keywords: CP/M, DOS, Linux, Macintosh, Microcomputers, OS/2, Operating Systems, Small Computer Systems, Windows, Windows NT

8 Digital test generation and design for testability
John Grason, Andrew W. Nagle
June 1980 **Proceedings of the 17th conference on Design automation**
Publisher: ACM Press
Full text available: ⬚ pdf(1.42 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

This paper is a tutorial intended primarily for individuals just getting started in digital testing. Basic concepts of testing are described, and the steps in the test development process are discussed. A pragmatic approach to test sequence generation is presented, oriented towards ICs interconnected on a board. Finally, design for testability techniques are described, with an emphasis on solving problems that appeared during the test

generation discussion.

9 Operational features of an MOS timing simulator
P. Kozak, H. K. Gummel, B. R. Chawla
January 1975 **Proceedings of the 12th conference on Design automation**
Publisher: IEEE Press

Full text available: pdf(524.38 KB)   Additional Information: full citation, abstract, references, citings, index terms

This paper describes operational features of a timing simulator having performance characteristics between those of circuit analysis programs and conventional logic simulators.

10 Novanet communications network for a control system
J. R. Hill, J. R. Severyn, P. J. VanArsdall
October 1983 **ACM SIGCOMM Computer Communication Review , Proceedings of the eighth symposium on Data communications SIGCOMM '83**, Volume 13 Issue 4
Publisher: ACM Press

Full text available: pdf(1.07 MB)   Additional Information: full citation, abstract, references, index terms

Novanet is a control system oriented fiber optic local area network that was designed to meet the unique and often conflicting requirements of the Nova laser control system which will begin operation in 1984. The computers and data acquisition devices that form the distributed control system for a large laser fusion research facility need reliable, high speed communications. Both control/status messages and experimental data must be handled. A subset of NOVANET is currently operating on the ...

11 Verifying large-scale multiprocessors using an abstract verification environment
Dennis Abts, Mike Roberts
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Publisher: ACM Press

Full text available: pdf(160.82 KB)   Additional Information: full citation, abstract, references, index terms

Due to a patent dispute, full text of this article is not available at this time.

12 Left to its own devices, APL plots on the bus
Curtis A. Jones
July 1992   **ACM SIGAPL APL Quote Quad , Proceedings of the international conference on APL APL '92**, Volume 23 Issue 1
Publisher: ACM Press

Full text available: pdf(736.86 KB)   Additional Information: full citation, abstract, references, index terms

The IEEE-488 General-Purpose Interface Bus is a convenient vehicle through which APL can run a variety of devices and computers. This paper shows how a PC can be used with APL as a device on the bus, in contrast to the PC's more usual role as system controller. As an example, an APL workspace that emulates an x-y plotter attached to the GPIB is shown. This illustrates the GPIB providing input to an APL workspace, and techniques by which APL can report the status of the devi ...

13 The Alpha demonstration unit: a high-performance multiprocessor
Charles P. Thacker, David G. Conroy, Lawrence C. Stewart
February 1993 **Communications of the ACM**, Volume 36 Issue 2
Publisher: ACM Press

Full text available: pdf(6.26 MB)   Additional Information: full citation, references, citings, index terms, review

Keywords: Alpha AXP chip

14 Virtual machine monitors: Xen and the art of virtualization

Paul Barham, Boris Dragovic, Keir Fraser, Steven Hand, Tim Harris, Alex Ho, Rolf
Neugebauer, Ian Pratt, Andrew Warfield
October 2003 **Proceedings of the nineteenth ACM symposium on Operating systems
principles**
Publisher: ACM Press

Full text available: pdf(168.76 KB)   Additional Information: full citation, abstract, references, citings, index
terms

Numerous systems have been designed which use virtualization to subdivide the ample
resources of a modern computer. Some require specialized hardware, or cannot support
commodity operating systems. Some target 100% binary compatibility at the expense of
performance. Others sacrifice security or functionality for speed. Few offer resource
isolation or performance guarantees; most provide only best-effort provisioning, risking
denial of service.This paper presents Xen, an x86 virtual machine monit ...

Keywords: hypervisors, paravirtualization, virtual machine monitors

15 Vax Station: A General-Purpose Raster Graphics Architecture

H. M. Levy
January 1984 **ACM Transactions on Graphics (TOG)**, Volume 3 Issue 1
Publisher: ACM Press
Full text available: pdf(1.16 MB)   Additional Information: full citation, references, citings, index terms

16 QCDSP: a Teraflop scale massively parallel supercomputer

Dong Chen, Ping Chen, Norman H. Christ, Robert G. Edwards, George Fleming, Alan Gara,
Sten Hansen, Chulwoo Jung, Adrian Kahler, Stephen Kasow, Anthony D. Kennedy, Greg
Kilcup, Yu Bing Luo, Catalin Malureanu, Robert D. Mawhinney, John Parsons, Jim Sexton,
ChengZhong Sui, Pavlos Vranas
November 1997 **Proceedings of the 1997 ACM/IEEE conference on Supercomputing
(CDROM)**
Publisher: ACM Press
Full text available: pdf(85.03 KB)   Additional Information: full citation, abstract, references

We discuss the work of the QCDSP collaboration to build an inexpensive Teraflop scale
massively parallel computer suitable for computations in Quantum Chromodynamics
(QCD). The computer is a collection of nodes connected in a four dimensional toroidial
grid with nearest neighbor bit serial communications. A node is composed of a Texas
Instruments Digital Signal Processor (DSP), memory, and a custom made communications
and memory controller chip. An 8192 node computer with a peak speed of 0.4 Ter ...

Keywords: QCD, digital signal processor, parallel, supercomputer

17 Porting AIX onto the student electronic notebook

John Ioannidis, Gerald Q. Maguire, Israel Ben-Shaul, Marios Levedopoulos, Micky Liu
May 1991 **Proceedings of the 1991 ACM SIGSMALL/PC symposium on Small systems**
Publisher: ACM Press

Full text available: pdf(755.19 KB)　Additional Information: full citation, references, index terms

18 Web-based remote manipulation in advanced manufacturing system
Dan Zhang, Lihui Wang
March 2005 **Proceedings of the IEEE EEE05 international workshop on Business services networks BSN '05**
Publisher: IEEE Press
Full text available: pdf(350.07 KB)　Additional Information: full citation, abstract, references

> In this paper, a Web-based collaborative framework is proposed. With appropriate open architecture for effective collaboration among a dispersed engineering team, the Web-based digital Shop Floor can serve real-time data from bottom up and can function as a constituent component of e-manufacturing for remote monitoring and control. This paper presents the basis of the framework for building web-based collaborative systems that can be used for distributed manufacturing. A proof-of-concept protototy ...

19 Connecting a minicomputer to an X.25 network: a case study
Andrzej Ciepielewski, Thomas Jungefeldt, Jan Linnéll
January 1983 **ACM SIGCOMM Computer Communication Review**, Volume 13 Issue 1
Publisher: ACM Press
Full text available: pdf(935.95 KB)　Additional Information: full citation, references

20 OMP: a RISC-based multiprocessor using orthogonal-access memories and multiple spanning buses
K. Hwang, M. Dubois, D. K. Panda, S. Rao, S. Shang, A. Uresin, W. Mao, H. Nair, M. Lytwyn, F. Hsieh, J. Liu, S. Mehrotra, C. M. Cheng
June 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th international conference on Supercomputing ICS '90**, Volume 18 Issue 3b
Publisher: ACM Press
Full text available: pdf(1.96 MB)　Additional Information: full citation, abstract, references, citings, index terms

> This paper presents the architectural design and RISC based implementation of a prototype supercomputer, namely the Orthogonal MultiProcessor (OMP). The OMP system is constructed with 16 Intel 1860 RISC microprocessors and 256 parallel memory modules, which are 2-D interleaved and orthogonally accessed using custom-designed spanning buses. The architectural design has been validated by a CSIM-based multiprocessor simulator. The design choices are based on worst-case delay a ...

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